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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,599	02/01/2001	Bruno Couillard	47-09 US	3830

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EXAMINER	
DADA, BEEMNET W	

ART UNIT	PAPER NUMBER
2135	3

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/774,599	COUILLARD, BRUNO	
	Examiner	Art Unit	
	Beemnet W Dada	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Petivan et al. (hereinafter Petivan) (US Patent No. 6,141,769).

4. As per claim 19, Petivan teaches a method for verifying an on-board clock device to compensate for individual deviation comprising the steps of:

receiving a signal including a plurality of time synchronization values at each of a plurality of modules [column 5, lines 39-45 and column 10, lines 47-67]; and

each module determining a synchronization status of itself and, upon determining a status other than in synchronization with the other modules, disabling itself [column 10, lines 47-67 and column 16, lines 47-63].

5. As per claim 20, Petivan teaches the method as applied to claim 19 above. Furthermore, Petivan teaches providing by each module a value representative of a time associated with that module to each other module of the plurality of modules [column 5, lines 39-45].

6. As per claim 21, Petivan teaches the method as applied to claim 20 above. Furthermore, Petivan teaches the method, wherein the signal including a plurality of time synchronization values received at each module includes a tally of modules that are synchronized with that module and a tally of modules that are other than synchronized to that module, said tallies used by each module to determine its synchronization status [column 10, lines 47-67].

7. As per claim 22, Petivan teaches the method as applied to claim 21 above. Furthermore, Petivan teaches the method, wherein each module determines its synchronization status in dependence upon receiving data indicative of a predetermined minimum fraction of modules being in synchronization therewith [column 10, lines 47-67 and column 12, Section 3.5].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 18, 23, 24, 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petivan et al (US Patent No. 6,141,769) in view of Fischer (US Patent No. 6,408,388 B1).

10. As per claim 1, Petivan teaches a method for updating an on-board clock device to compensate for individual deviation from a time value comprising the steps of:

a) providing a signal from each of a plurality of modules indicating a time associated with said module and for use by said module [column 5, lines 39-45 and column 10, lines 47-67];

b) receiving the signal from each of the plurality of modules and determining a synchronization between the modules to detect synchronized modules and modules that are other than synchronized with the synchronized modules [column 5, lines 39-45 and column 10, lines 47-67]; and,

c) when a module is detected as other than synchronized with the synchronized modules, automatically performing one of synchronizing that module with the synchronized modules and disabling that module from performing operations [column 16, lines 47-67].

Petivan does not explicitly teach the plurality of modules performing time stamping operations. However, Fischer teaches a method of performing time stamping operations [column 1, lines 67-67 and column 2, lines 1-15]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a time stamping operations as per teachings of Fischer and include it into the synchronized plurality of modules taught by Petivan in order to perform time stamping operations at a user device, using synchronized plurality of modules that perform time operations and eliminating the need for separate time stamping operation at a remote location.

11. As per claims 23 and 24, Petivan teaches, a method for inserting a new module comprising the steps of:

a) installing a module within a communication bus [column 6, lines 59-66];

b) detecting the module and synchronizing the module by setting the real time clock of the module in dependence upon a value indicative of a current time from the real time clocks of other modules, wherein the step of detecting the module is performed in response to the module providing a signal indicative of a non-synchronized status of the module [column 11, lines 1-4]. Petivan does not explicitly teach the plurality of modules performing time stamping operations. However, Fischer teaches a method of performing time stamping operations [column 1, lines 67-67 and column 2, lines 1-15]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a time stamping operations as per teachings of Fischer and include it into the synchronized plurality of modules taught by Petivan in order to perform time stamping operations at a user device, using synchronized plurality of modules that perform time operations and eliminating the need for separate time stamping operation at a remote location.

12. As per claims 26 and 29, Petivan teaches a module comprising:

a real time clock for providing a time measurement for time [column 5, lines 27-33];

a microprocessor connected to the real time clock for handling at least a processing function for periodically updating the real time clock [column 5, lines 51-67];

a secure port in electrical communication with the microprocessor for exchanging information with a device external to the module, wherein the secure port is for mating with a corresponding port of a secure communication bus to provide a secure communication channel for exchanging a value which is characteristic of a time of day with a second other module

mated with a second other corresponding port of a same secure communication bus for at least a same overlapping period of time (i.e., I/O port for exchanging time of day information with other modules through I/O buses) [column 3, lines 1-35] ; and,

a lock for enabling the module in a first state and for disabling the module in a second other state (i.e. synchronized state and disabling a module when detected as unsynchronized with other modules) [column 10, lines 47-67].

Petivan does not explicitly teach the plurality of modules performing time stamping operations. However, Fischer teaches a method of performing time stamping operations [column 1, lines 67-67 and column 2, lines 1-15]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a time stamping operations as per teachings of Fischer and include it into the synchronized plurality of modules taught by Petivan in order to perform time stamping operations at a user device, using synchronized plurality of modules that perform time operations and eliminating the need for separate time stamping operation at a remote location.

13. As per claim 2, the combination of Petivan and Fischer teaches the method as applied to claim 1 above. Furthermore, Petivan teaches the method, wherein each module of the plurality of modules is inserted within a same module housing for at least a same overlapping period of time, the module housing electrically connected to a computer system and for providing communication between each module of the plurality of modules and between the plurality of modules and the computer system [column2, lines 65-67, column 3, lines 1-17 and figure 3].

14. As per claim 18, the combination of Petivan and Fischer teaches the method as applied to claim 1 above. Furthermore, Petivan teaches the method further comprising disabling the

detected module and synchronizing the detected module with other modules [column 16, lines 47-67].

15. As per claim 27 and 30, the combination of Petivan and Fischer teaches the module as applied above. Furthermore, Petivan teaches the module further comprising an on-board power source for maintaining at least an initialization status [column 6, lines 1-15].

16. As per claim 28, the combination of Petivan and Fischer teaches the module as applied above. Furthermore, Petivan teaches the module further comprising disabling a failed module and synchronizing the failed module with other modules [column 16, lines 47-67].

17. Claims 3-17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petivan (US Patent No. 6,141,769) in view of Fischer (US Patent No. 6,408,388 B1) as applied to claims 1, 2 and 24 above, and further in view of Lewis (US Patent No. 5,734,819).

18. As per claims 3 and 25, the combination of Petivan and Fischer teaches synchronizing plurality of modules for performing time stamping operations and as applied to claims 1, 2 and 24 above. The combination of Petivan and Fischer does not explicitly teach authentication of modules. However Lewis teaches authentication of modules in a computer system [column 1, lines 60-65 and column 2, lines 1-13]. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of module authentication taught by Lewis within the method of synchronizing plurality of modules for time stamping operations taught by the combination of Petivan and Fischer in order to protect

modules and communications between modules from unauthorized access and modification by applying authentication between synchronized modules.

19. As per claims 4, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Petivan teaches the method further comprising disabling that module that is other than synchronized with the synchronized modules by erasing data stored within that module (disabling the detected module and synchronizing the detected module with other modules, taking the detected module of-line, and restoring information after re-synchronization) [column 6, lines 59-67 and column 16, lines 47-67].

20. As per claim 5, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Petivan teaches the method further comprising disabling that module that is other than synchronized with the synchronized modules by erasing data stored within that module (disabling the detected module and synchronizing the detected module with other modules, taking the detected module of-line, and restoring information after re-synchronization) [column 6, lines 59-67 and column 16, lines 47-67].

21. As per claims 6 and 7, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Petivan teaches the method further comprising disabling the module other than synchronized with the synchronized modules, setting a flag and preventing operation of the module from operations [column 16, lines 47-67 and column 6, lines 42-46]

22. As per claim 8, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Petivan teaches the method further comprising:

initializing the detected module, sending a new value characteristic of a current time of day to said module, and setting the real time clock of said module in dependence upon the received new value (restoring information into the detected module and re-synchronization the detected module with synchronized modules) [column 6, lines 59-67].

23. As per claim 9 the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Fischer teaches a master clock for synchronizing other clocks [column 4, lines 46-59].

24. As per claims 10, the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Lewis teaches authentication of modules [column 1, lines 60-65 and column 2, lines 1-13].

25. As per claim 11, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Lewis teaches providing authentication signal from different modules for authentication [column 1, lines 45-57].

26. As per claim 12, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Lewis teaches encryption communications between modules using message authentication coed (MAC) [column 2, lines 7-20], because the method further protects modules and communications between modules from unauthorized access and modification by applying encryption between synchronized modules.

27. As per claim 13, the combination of Petivan, Fischer and Lewis teaches the method as applied above. Furthermore, Fischer teaches synchronizing at predetermined intervals [column 4, lines 55-59].

28. As per claims 14, the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Fischer teaches a master clock for synchronizing other clocks in a device at a particular interval [column 4, lines 55-60].

29. As per claims 15, the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Lewis teaches encryption communications between modules using message authentication coed, and storing data between modules in memory [column 2, lines 7-20], because the method further protects modules and communications between modules from unauthorized access and modification by applying encryption between synchronized modules.

30. As per claim 16, the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Fischer teaches a master clock synchronizing other clocks [column 4, lines 55-65].

31. As per claim 17, the combination of Peitvan, Fischer and Lewis teaches the method as applied above. Furthermore, Lewis teaches encryption communications between modules [column 2, lines 7-20], because the method further protects modules and communications between modules from unauthorized access and modification by applying encryption between synchronized modules.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Beemnet W Dada whose telephone number is (703) 305-8895. The examiner can normally be reached on Monday - Friday (8:30 am - 6:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Beemnet Dada

AU 2135

June 18, 2004